Engineering Tripos Part IIA Project, SB1: VLSI Design, 2018-19

Leader

Dr D M Holburn [1]

Timing and Structure

Fridays 9-11am, plus afternoons and Tuesdays 11-1pm

Prerequisites

3B1 & 3B2 very useful, Part IB Electrical Engineering Selected Topic helpful

Content

This project offers the unique experience of the full spectrum of activities undertaken by a professional IC designer. This is achieved through the design of a small ?system-on-a-chip?, right to the point where it could be sent to a foundry for manufacture.

The project will begin with an introduction to the structure of MOS integrated circuits and the related design concepts. The importance of physical dimensions and design rules as fundamental elements in the design process will be illustrated using directed exercises.

The Mentor Graphics ICstudio design suite will be introduced through exercises in schematic capture and circuit simulation. The importance of hierarchy in IC design will be illustrated by developing a hierarchical design using cells drawn from a library of digital and analogue elements. Methods of high-level functional design synthesis based on hardware description languages (VHDL) will also be explored(Modelsim).

IC layout will be introduced through the examination of the layout of a simple two-input logic gate. This will be adapted and its layout modified to produce an efficient and high speed design(ICstation). This activity will also introduce the key mask layers and the tools available (ICrules) for detecting design rule violations. Techniques for interconnecting complex structures using metal and polysilicon layers will be explored. Methods for functional verification of the circuit will then be investigated, using dedicated tools for extracting netlists and parametric values from layout. These will be compared against a standardised set drawn from a circuit schematic (ICtrace). Tools for numerical modelling (Eldo) will be used to assess the transfer characteristic and transient response of the test design. The effects of varying device geometry on performance will be illustrated in this way. Simulated performance will be compared with measurements made on a design fabricated in an earlier project.

These approaches to design will then be combined in the implementation and verification of a more complex system, incorporating counters, dividers, control logic and, where appropriate, analogue circuit elements, augmented by a number of additional library cells, including the two-input gate laid out during the project. The development will continue to the point where a complete design is produced, ready for shipping to a silicon foundry for fabrication.

FORMAT

Students will work in pairs, sharing the development of the design, but writing individual reports. Parts of the development will be carried out individually and merged in the final design.

Week 1

Development of design. Familiarisation with schematic design capture, hardware description and functional simulation tools. First interim report.

Week 2

Layout and design rule verification of logic gate structure. Measurement of characteristics of a real ring oscillator. Second interim report.

Week 3

Netlist extraction and modelling of logic gate design. Refinement of design.

Weeks 4

Implementation of system-on-a-chip embodying contributions from each participantdesign, with verification carried out according to the techniques encountered in earlier sessions. Final report.

MINI-LECTURES

1.Introduction to VLSI Design. The ring oscillator.

2.Integrated Circuit Layout techniques

Circuit to be designed

After successfully completing the introductory exercises, students will first undertake a design including a ring oscillator, using a chain of inverting logic gates. A compact layout free from design rule violations, with the highest possible oscillation frequency will be the objectives. This will be used as a component in a more elaborate digital design, or ?system-on-a-chip?, which will embody contributions from each participant. The target design will be described in the project manual.

Methods to be employed

Where necessary, student performance will be judged on the basis of: the extent to which the design meets the project specification, the compactness and freedom from violations of the layout, and the quality of the simulation results and other material presented in the interim and final reports.

Coursework

Coursework	Due date	Marks
Interim report 1	Thu 16 May 2019	15
Interim report 2	Thu 23 May 2019	15
Final report	4pm, Friday 7 June 2019	25

Examination Guidelines

Please refer to Form & conduct of the examinations [2].

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Links
[1] mailto:dmh14@cam.ac.uk
[2] https://teaching22-23.eng.cam.ac.uk/content/form-conduct-examinations